



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,167	09/30/2003	Cetin Kaya	TI-24995.1	5903

23494 7590 09/29/2004

TEXAS INSTRUMENTS INCORPORATED  
P O BOX 655474, M/S 3999  
DALLAS, TX 75265

EXAMINER
----------

TRINH, MICHAEL MANH

ART UNIT	PAPER NUMBER
----------	--------------

2822

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/675,167

Applicant(s)

KAYA ET AL.

Examiner

Michael Trinh

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 September 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 11-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 11-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

Art Unit: 2822

## **DETAILED ACTION**

\*\*\* This office action is in response to Applicant's Pre-amendment filed on September 30, 2003. Claims 1-10 were canceled. Claims 11-15 are pending.

### ***Specification Objection***

1. The specification page 8, line 7, mentions "...but prior to prior to performing any other steps...", but it is unclear from the description for what are "any other steps" (e.g. which of any other steps are not excluded). Note that since the specification teaches "...only two layers are present between the first layer of silicon and the second layer of silicon...", it is apparently meant prior to performing any other layers. Clarification and correction is respectfully requested.

### ***Claim Rejections - 35 USC § 112***

2. Claims 11-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 11, as already described above under the specification objection, meaning and scope of "...prior to performing any other steps..." in base claim 11 are unclear and indefinite for what are "any other steps", wherein the specification does not define what other steps are excluded. Is it meant prior to performing any other layers?

(Depending claims are rejected as depending on rejected base claim)

\*\* Insofar as understood, the claims are rejected as below:

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Art Unit: 2822

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 11-12 rejected under 35 U.S.C. 102(b) as being anticipated by Schlais et al (5,014,098).

Schlais et al teach (at Figs 14-18; col 8) a method comprising at least the steps of: forming a first layer of silicon 54 at least partially overlying substantially monolithic body of semiconductor material 18; forming a layer of nitride 58 at least partially overlying said first layer of silicon 54; forming a layer of oxide 56 at least partially overlying said first layer of silicon 54 (Figs 17,18,16; col 8, lines 25-45); after said steps of forming said layer of nitride and forming said layer of oxide, but prior to performing any other steps, forming a second layer of silicon 60 at least partially overlying said layer of oxide 56, said layer of nitride 58, and said first layer of silicon 54; wherein only two layers 58/56 are present between the first layer of silicon 54 and said second layer of silicon 58. Re claim 12, wherein before the layer of nitride 58, the layer of oxide 56 is formed (Figs 17-17; col 8, lines 25-40).

5. Claims 11,12,14 are rejected under 35 U.S.C. 102(e) as being anticipated by Kobayashi et al (6,489,649).

Kobayashi et al teach (at Figs 13a-14d; col 13, line 10 through col 14) a method comprising at least the steps of: forming a first layer of silicon 204 at least partially overlying substantially monolithic body of semiconductor material 201 (col 13, lines 11-34; Fig 13); forming a layer of nitride 213 at least partially overlying said first layer of silicon 204 (Fig 13d); forming a layer of oxide 205 at least partially overlying said first layer of silicon 204 (Fig 13c; col 13, lines 35-50); after said steps of forming said layer of nitride and forming said layer of oxide, but prior to performing any other steps, forming a second layer of silicon 207 at least partially overlying said layer of oxide 205, said layer of nitride 213, and said first layer of silicon 204 (Fig 14a-14d; col 13, lines 50-67); wherein only two layers are present between the first layer of silicon 204 and said second layer of silicon 207. Re claim 12, wherein before the layer

Art Unit: 2822

of nitride 213, the layer of oxide 205 is formed (Figs 13c-13d; col 13, lines 35-50). Re claim 14, wherein the layer of oxide 205 is deposited by LPCVD (col 13, lines 35-40).

6. Claims 11,13,15 are rejected under 35 U.S.C. 102(b) as being anticipated by Clementi et al (5,600,166).

Clementi et al teach (at Figs 2-8; col 5, line 25 through col 6) a method comprising at least the steps of: forming a first layer of silicon 5 at least partially overlying substantially monolithic body of semiconductor material 1 (col 5, lines 25-44); forming a layer of nitride 6a,b at least partially overlying said first layer of silicon 5 (Fig 4; col 4, lines 10-18; col 5, lines 45-65); forming a layer of oxide 6c at least partially overlying said first layer of silicon 5 (Fig 5; col 5, lines 45-65; col 6); after said steps of forming said layer of nitride and forming said layer of oxide, but prior to performing any other steps, forming a second layer of silicon 7 at least partially overlying said layer of oxide 6c, said layer of nitride 6a,b, and said first layer of silicon 5; wherein only two layers of nitride and oxide are present between the first layer of silicon 5 and said second layer of silicon 7. Re claim 13, wherein said layer of nitride 6a,b is formed before said layer of oxide 6a (Fig 4; col 5, lines 45-65). Re claim 15, wherein said layer of nitride 6a,b is thermally grown (col 5, lines 45-65).

### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Art Unit: 2822

8. Claims 11-13,15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneoka (6,344,394).

Kaneoka teaches a method comprising at least the steps of: forming a first layer of silicon 14,5 at least partially overlying a body of semiconductor material 1 (Figs 2a-2c; col 4; col 2, line 55 through col 3, line 16 ); forming a layer of nitride 6 at least partially overlying said first layer of silicon 14,5 (Fig 2c; col 4, lines 48-51); forming a layer of oxide 15,7 at least partially overlying said first layer of silicon 5,14 (Figs 2d-e; col 4, lines 52-55); after said steps of forming said layer of nitride 6 and forming said layer of oxide 15,7, but prior to performing any other steps, forming a second layer of silicon 8 (col 4, lines 61-67) at least partially overlying said layer of oxide 7,15, said layer of nitride 6, and said first layer of silicon 5,14; wherein only two layers are present between the first layer of silicon 5,14 and said second layer of silicon 8. Re claim 12, wherein before the layer of nitride 6, the layer of oxide 18 is formed (Figs 4c-4d; col 6, lines 22-40; Figs 4a-f; col 6, lines 7-64). Re claim 13, wherein said layer of nitride 6 is formed before said layer of oxide 15,7 (Figs 2c-2e; col 4, lines 48-60) 14. Re claim 15, wherein the layer of nitride 6 is thermally grown (col 2, line 55 through col 3, line 16; col 4, lines 49-51).

Kaneoka already teaches forming a first silicon layer 14 on a body of semiconductor material 1 for nonvolatile memory, but lacks mentioning a substantially monolithic body of semiconductor material.

However, Schlais teaches (at col 4, lines 23-30; Figs 16-18) using a single crystalline silicon 18 (i.e. a substantially monolithic silicon) for the body of semiconductor material 18 for forming a plurality of devices, wherein a first silicon layer 54 is formed on the single crystalline silicon body 18, wherein only two layers 56/58 of nitride and oxide are formed between a first and second silicon layers 54/60 for the nonvolatile memory.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the nonvolatile memory of Kaneoka in the substantially monolithic body of semiconductor material (e.g. single crystalline silicon) as taught by Schlais. This is because of the desirability to form the nonvolatile memory in a bulk single crystalline silicon body as a starting material, wherein the single crystalline silicon has a uniformity of crystal structure with a

Art Unit: 2822


high degree of crystalline perfection of single crystalline so that wherein the plurality of devices can be formed on the same body of single crystalline silicon.

\*\*\*\*\*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.  
Oacs-7

  
Michael Trinh  
Primary Examiner